

WHAT IS CLAIMED IS:

1. A semiconductor device, in which a semiconductor chip is connected to a wired substrate, comprising:

a through opening provided at a predetermined position  
5 of said wired substrate;

an under-fill region as a gap portion between said wired substrate and said semiconductor chip; and

a molded resin portion as peripheral portion along side edge of said semiconductor chip;

10 said molded resin portion and said through opening being sealed by resin;

a region where a distance between a connection surface with said semiconductor chip of said wired substrate and a resin surface of said molded resin portion is greater than a distance  
15 between said connection surface with said semiconductor chip of said wired electrode and a back surface of said semiconductor chip, being formed in said molded resin portion.

2. A semiconductor device, in which a semiconductor chip  
20 is connected to a wired substrate, comprising:

a through opening provided at a predetermined position of said wired substrate;

an under-fill region as a gap portion between said wired substrate and said semiconductor chip; and

25 a molded resin portion as peripheral portion along side

edge of said semiconductor chip;

said molded resin portion and said through opening being sealed by resin;

a stepped down portion as a recessed portion being formed  
5 surrounding said semiconductor chip in said molded resin portion as peripheral portion of said semiconductor chip.

3. A semiconductor device as set forth in claim 2, wherein said stepped down portion of said molded resin portion has a  
10 tilted surface descending from an upper end surface of said semiconductor chip.

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4. A semiconductor device as set forth in claim 1 or 2, wherein said molded resin portion is formed with an over-hang portion  
15 overlapping with the upper end surface of said semiconductor device.

5. A semiconductor device as set forth in claim 1 or 2, wherein said molded resin portion is formed over substantially entire  
20 area of said wired substrate.

6. A semiconductor device as set forth in claim 1 or 2, wherein said resin is injected through one or more through holes provided in said wired substrate for electrical connection under pressure  
25 for forming said under-fill region and said molded resin portion.

7. A resin seal process of a semiconductor device for sealing a molding object, in which a semiconductor chip is connected with a wired substrate by a flip chip connection, by way of a transfer sealing method, comprising steps of:

- 5        setting said molding object within a mold;  
         clamping said mold;

         injecting a resin into said resin flow passage provided in said mold for filling said resin through a through opening provided in said wired substrate from said resin flow passage  
10       for forming into a predetermined shape.

8. A resin seal process of a semiconductor device as set forth in claim 7, wherein filling of said resin is performed with varying injection amount of the resin per unit period  
15       according to elapsed time.

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9. A resin seal process of a semiconductor device as set forth in claim 7 or 8, wherein a plurality of said through openings and said resin flow passages are provided for performing filling  
20       of the resin at a plurality of portions.

10. A resin seal process of a semiconductor device as set forth in claim 9, wherein filling of resin from said plurality of portions is performed with setting filling speed per route  
25       of said resin flow passages independently of each other.

11. A resin seal process of a semiconductor device as set forth in claim 9, wherein filling of resin from a plurality of portions is performed with setting filling start timing per route of said resin flow passage independently of each other.

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12. A resin seal process of a semiconductor device as set forth in claim 9, wherein filling speed of resin into an under-fill region as a gap portion between said wired substrate and said semiconductor chip is lower than a filling speed of said resin into a molded resin portion as peripheral portion of said semiconductor chip.

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13. A resin seal process of a semiconductor device as set forth in claim 9, wherein filling timing of resin into an under-fill region as a gap portion between said wired substrate and said semiconductor chip is earlier than a filling timing of said resin into a molded resin portion as peripheral portion of said semiconductor chip.

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14. A resin seal process of a semiconductor device as set forth in claim 7 or 8, wherein filling of said resin is performed through one or more through holes provided in said wired substrate for electrical connection.

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15. A resin seal process of a semiconductor device as set

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forth in claim 7 or 8, which comprises step of setting a plurality of molding objects within the mold and clamping said mold for filing said resin for a plurality of semiconductor chips simultaneously.

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16. A resin sealing apparatus for resin sealing a molding object, in which a semiconductor chip is connected to said mold and a resin seal is formed in a shape of a cavity portion provided in said mold by a transfer seal method, comprising:

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a resin flow passage formed as a space in said mold up to a position corresponding to a through opening provided in a wired substrate from a plunger introducing opening for performing injection of the resin into said mold.

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17. A resin sealing apparatus as set forth in claim 16, wherein a plurality of said resin flow passages are provided and volumes of respective resin flow passages are provided per route.

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18. A resin sealing apparatus as set forth in claim 16 or 17, wherein said mold is consisted of an upper die, an intermediate die and a lower die,]

said lower die has a cavity portion as a die for outer shape of a molded resin portion of said semiconductor device;

said intermediate die is exchangeably arranged a gate plate formed with a resin injection conduit as a hole formed

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said upper die is formed with a runner as a groove extending to a position corresponding to said resin injection conduit; and

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20. A resin sealing apparatus as set forth in claim 16 or 17, wherein said mold is formed with a stepped down portion recessed with a tilted peripheral portion of said cavity portion in a region corresponding to the semiconductor chip.